REMARKS

STATUS OF THE CLAIMS

In accordance with the foregoing, claims 1and 3-5 have been amended. Claim 2 has been cancelled. New claims 6-8 have been added. Claims 1 and 3-8 are pending and under consideration.

No new matter is being presented, and approval of the amended claims is respectfully requested.

REJECTIONS OF CLAIMS 1 AND 2 UNDER 35 U.S.C. §102(b) AS BEING ANTICIPATED BY OSAKA ET AL. (U.S. PATENT NO. 5,787,261)

Dependant claim 2 is cancelled herein; however, the features thereof are incorporated into independent claim 1. The rejection of claim 1 is respectfully traversed and reconsideration is requested.

An object of the present invention of independent claim 1 is that when an active connection of a device unit is made, the influence of noise on another device unit or device connected to the same data bus is eliminated. As another object, the present invention prevents device units of a self system and other systems from malfunctioning when glitch noise that occurs in making an active-line connection or disconnection of a functional circuit board (device unit), with respect to a data transfer bus (data bus), propagates to the device units.

That is, independent claim 1 relates to a timing design method in which the propagation of glitch noise occurring by active-line insertion, the time transition of a control signal of a bus switch, and the skew of a timing-signal are used as parameters. On the basis of these parameters, the timing at which glitch noise, occurring by active-line insertion, reaches device units of self and other systems is computed, thereby preventing a malfunction that occurs when these device units infringe a setup time at the time of synchronous operations.

On page 7 of the Action, the Examiner states that Osaka et al. (hereinafter "Osaka") discloses computing timing at which, when each one of said plurality of device units is connected on said data bus being active, noise propagates to the other one of said plurality of device units or to the other device connected on said data bus (citing Osaka column 8, lines 22-38, column 8, line 60, to column 9, line 7, and column 12, line 45, to column 14, line 38).

However, Osaka describes an active-line inserting/withdrawing system in which the pre-charge resistor is connected in parallel with the switching element for performing clock synchronization control and in close proximity to a connector, and before electrically connecting

the functional circuit board to a data transfer bus by operation of the switching element, a difference in potential between the data transfer bus and a signal path in the functional circuit board is minimized through the pre-charge resistor. Thereby, glitch noise that occurs at the time of active-line insertion is suppressed.

Thus, in Osaka, by preventing noise from occurring on the data transfer bus, when the functional circuit board is inserted in the data transfer bus with signal lines remaining in an active state, glitch noise is prevented from propagating to other functional circuit boards through the data transfer bus of a bus and causing malfunctions.

Further, the Examiner states on page 3 of the Action that Osaka teaches the insertion of glitch noise on the bus line because the suppression of the glitch noise will not completely prevent the insertion of any glitch noise, but rather, reduces the glitch noise inserted to a small amount that would be acceptable without causing a malfunction to the system. Thus, it appears that the Examiner understands that Osaka is directed to merely preventing noise from occurring on the data transfer bus.

In contrast, embodiments of the present invention disclose computing the timing at which glitch noise propagates to the device units of other systems connected to the data bus by active-line insertion.

Further, regarding dependent claim 2, the Examiner states that Osaka teaches computing a delay time "b", citing DELTAt 50 of Fig. 8 and column 13, line 8, to column 14, line 38, of Osaka. However, the delay time "b" according to claim 2 is needed for said bus switch to connect each one of said plurality of devices units on said data bas after each one of said plurality of bus device units is connected on said timing-signal bus. In contrast, DELTAt of Osaka is merely the delay time of the bus clock signal 41 controlled by the switch controller 14 within an element (device) 3 that can be inserted or withdrawn to/from the bus. Thus, DELTA t has no relation to delay time necessary dependent upon computed timing for noise to propagate to the other one of said plurality of device units.

Therefore, it is respectfully submitted that independent claim 1, as amended, patentably distinguishes over the prior art.

REJECTIONS UNDER 35 U.S.C. §103(a)

Claims 3-5 are rejected for obviousness as being unpatentable over Osaka. The rejections are respectfully traversed and reconsideration is requested.

Independent claims 4 and 5 recite similar features to those described above. Thus, the foregoing arguments are also submitted for independent claims 4 and 5.

Furthermore, it is noted that an important feature of claims 3-5 is that a timing margin M {= (T + g) – (a + b + c + d + e + f) – S} from arrival of said noise at the other of said plurality of device units or the one or more other devices to start of said setup time is 0 or greater, and the delay time "b" of the bus switch is computed so that the timing margin M is 0 or greater.

Thus, claims 3-5 recite a parameter "f" representing active-line insertion noise which propagates to other device units. That is, claims 3-5 are based on the premise that active-line insertion of a device unit causes noise to propagate to other devices.

On the other hand, Osaka discloses that Tclk < DELTAt + Tpzh + Tskew in which "Tclk" represents a bus cycle, DELTAt is a timing parameter for controlling a switching element 11 of a device unit which is inserted in a system being in its active state (active-line insertion of the device unit), "Tpzh" is the time required for a switching element 11 to electrically connect a bus 1 and a wiring 13 together from input of a switching control signal 42, and "Tskew" is the clock skew of the system.

Thus, Osaka discloses that by preventing DELTAt and the clock cycle from overlapping each other, and also preventing noise from occurring at the time of active-line insertion of a device unit by operation of a precharge resistance 12, the influence on other devices due to the active-line insertion is eliminated.

However, since Osaka fails to disclose the parameter "f" representing active-line insertion noise which propagates to other device units, Osaka is not based on the premise that noise propagates to other device units by the active-line insertion of a device unit.

Therefore, Osaka, in which the occurrence of noise is suppressed without taking into consideration noise propagating to other devices, does not disclose the aforementioned particularly important and significant features of claims 3-5.

As a result, it is respectfully submitted that dependent claim 3 and independent claims 4 and 5 patentably distinguish over the prior art. Moreover, dependent claim 3 depends from independent claims 1 and inherits the patentability thereof. Thus, it is further submitted that claim 3 patentably distinguishes over the prior art for the reasons provided above for independent claim 1.

NEW CLAIMS 6-8

Please note that the features of new dependent claims 6-8 can be found on page 22, lines 9-12, of the present specification.

New claims 6-8 depend from independent claims 1, 4 and 5, respectively, and inherit the patentable recitations thereof. Thus, it is respectfully submitted that claims 6-8 patentably

distinguish over the prior art for at least the reasons provided above. It is further submitted that the cited art of record fails to teach or suggest the features recited therein.

CONCLUSION

In accordance with the foregoing, it is respectfully submitted that all outstanding objections and rejections have been overcome and/or rendered moot. Further, all pending claims patentably distinguishes over the prior art. There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: March 12, 2007

By: Michael P. Stanley

Michael P. Stanley
Registration No. 58,523

1201 New York Avenue, N.W., 7th Floor
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501